LOW POWER CIRCUIT DESIGN FOR SRAM USING HETRO JUNCTION TUNNELING TRANSISTOR

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Abstract: The aim of this project is to design the 6T SRAM using SRAM and HETT. This project is carried out to investigate the performance and the characteristics of the SRAM. The 6T SRAM cell is selected cell to be design in this project due to higher performance of the cell compared with the other type of cell. The objectives of this study are to design the SRAM cell by using the TSPICE software in two operations in the 6T SRAM cells which are in the write and read operation. The operation time of each operation is observed and compared. The complete time taken for the read operation is higher than write operation. Then power dissipation in the write and read operation are calculated and discussed for various type of SRAMs during read and write operation. Finally 6T SRAM,7TSRAM and Schmitt trigger based 6T SRAM and 6T SRAM using adiabatic logic are designed and results are compared with its 4*4 SRAM array logic.

Keywords: HETT, memory, SRAM, TSPICE


I Introduction

Predictive Technology Model (PTM) provides accurate, customizable, and predictive model files are compatible with the standard circuit simulators, such as SPICE, and scalable with a wide range of process variations. With PTM, competitive circuit design and research can start even before the advanced semiconductor technology is fully developed.

SPICE is one of the types of Predictive Technology Model. There is a several type of SPICE such as TSPICE, PSPICE and the latest type is HSPICE. TSPICE is faster and has more capabilities than typical SPICE simulators. More time can be saved and it easy to detect the error if there is the problem in simulation process.

The Static Random Access Memory (SRAM) was created by using the TSPICE software. The circuit’s performance of SRAM will be obtained through TSPICE and the performance of circuit will be analyzed based on the waveform.

In this paper, we investigate circuit designs using the recently proposed Si/SiGe heterojunction tunneling transistor (HETT). The Si/SiGe heterostructure uses gate-controlledmodulation of band-to-band tunneling to obtain subthreshold swings of less than 30 mV/decade with a large ON current of 0.42 mA/μm at Vds = 0.5 V. Furthermore, Si/SiGe heterostructures are fully compatible with current MOSFET fabrication and can leverage the extensive prior investment in CMOS fabrication technology. Several industry and university teams have actively developed Si/SiGe HETT-type transistor structures, and initial devices have been experimentally demonstrated. We explore the key differences between HETTs and traditional MOSFETs that must be considered in the design of circuits using these new devices. Most significantly, HETTs display asymmetric conductance. In MOSFETs, the source and Drain are interchangeable, with the distinction only determined by the voltages during operation. However, in HETTs, the source and drain are determined at the time of fabrication, and the current flow for VDs < 0 is substantially less than for Vds > 0 [in an N-type HETT (NHETT)]. Hence, HETTs can be thought to operate unidirectionally, passing logic values only in one direction, which has significant implications on logic and especially static random access memory (SRAM) design.

II.Hett Device Characteristics

When the gate is biased positively, the device is turned on because electrons in the valence band of the p- type source can tunnel into the conduction band of the channel. If the Fermi level in the source is less than a few thermal voltages (kT) below the valence band edge, the bandgap acts as an “energy filter,” precluding tunneling from the exponential portion of the Fermi–Dirac distribution. If the gate bias is reduced sufficiently so that the bottom of the conduction band in the channel rises above the top of the valence band in the source, the tunneling abruptly shuts off. Because of this filtering of the Fermi–Dirac distribution function by the bandgap, the subthreshold slopes can be significantly smaller than 60 mV/decade.
A potential problem with tunneling transistors is that a very narrow bandgap semiconductor must be used to obtain sufficiently high ON current. However, narrow bandgap materials also lead to higher OFF currents, and are often incompatible with standard CMOS processing. To avoid this problem, a type-II HETT can instead be employed. In such a case, the source-to-body contact has a staggered band lineup that creates an effective tunneling band gap $E_{g eff}$, which is smaller than that of the constituent materials. Such a band structure can also be realized in the Si/SiGe heterostructure material system, and complementary N- and P-HETTs can be fabricated by reusing the masks for NFETs and PFETs, making this technology fully CMOS compatible. For optimized HETT drain, each device can require two more masks, and to get HETT optimized sources would take two more, resulting in 0–4 additional masks for HETT implementation depending on the degree of optimization. This is still far less than number of additional masks required for BiCMOS, which takes about eight extra masks. 

Fig. 2 shows a schematic diagram of a complementary Si/SiGe HETT technology.

For the circuit simulations in this paper, an optimized device structure was used. The simulated HETT devices have a gate length of 40 nm and a high-k gate dielectric with effective gate oxide thickness of 1.2 nm. For NHETT, the source consists of pure Ge, with 3% biaxial compressive strain, and Si channel with 1% biaxial tensile strain. The complementary P-type HETT (PHETT) design includes a strained Si source and pure Ge channel. Using band offsets from [15], the effective bandgap for this structure is 0.22 eV. For the transport calculations, a nonlocal tunneling model [16] with a twoband dispersion relationship within the gap was used. Effective masses are 0.17m₀ near the conduction band and 0.105m₀ near the valence band in the silicon channel, and 0.10m₀ near the conduction band and 0.055m₀ near the valence band in the pure Ge source [17].

The device has a 2-nm gate overlap of the source and an abrupt source doping profile. A gate work function of ~4.4 eV is used to set the OFF current to<1 pA/μm.

III.6t Sram Design With Hett

The asymmetric current flow of HETT places restrictions on the use of the pass gate and the transmission gate. This limitation is not severe for logic circuits since the CMOS logic, which is the most widely used logic, is not affected by this property because the current is expected to flow only in one direction in the channel of each transistor. Moreover, any pass-gate logic can be easily converted to CMOS logic to prevent malfunctions with HETT. However, the impact of HETTs asymmetric current flow on SRAM is significant since standard 6T SRAM uses pass gates for access transistors, which is not trivial to replace. In this section, we first analyze the implications of asymmetric current flow on SRAM operation and go on to propose an alternative 7T HETT-based SRAM cell topology. We then compare the 7T performance and robustness to that of a CMOS-based 6T SRAM design.
the write ability of the cell by making it more difficult to change the voltage at node N0. However, as shown in Fig. 15(b), since the pulldown current path (AXR) plays the major role in writing, the size ratio of AXR to PPUR, or AX to PPU, is the critical one for writeability and can be improved by increasing this ratio. This implies that, up to a point, readability and writeability in CMOS 6T SRAM can be improved individually at the cost of larger area.

IV. Alternative SRAM Design With Hett

Based on the previous discussion, 7T SRAM optimized for HETT is proposed as shown in Fig. 4. In this topology, readability/writeability tradeoffs in HETT-based 6T SRAM are overcome by utilizing separate read and write structures. The reduced 8T read enables extremely robust read with minimal additional number of HETT, and two-side NHETT pull-down write enables robust write with cell β-ratio of 1, where all HETT sizes can be minimum. There have been several 7T SRAM cell structure published earlier; however do not use decoupled read use two transistors as a decoupled read structure, and none of these prior artwork has used a single transistor decoupled read.

The HETT 7T SRAM is estimated to have <15% area overhead over a standard 6T, while the 8T SRAM exhibits 29% cell area overhead. In 7T SRAM, making the overhead for two 7T cells equal to that of one 8T cell. Moreover, as will be shown below, the 7T cell with all transistors at minimum size shows improved robustness over 6T at low voltage, hence if an up sized 6T were to use decoupled read use two transistors as a decoupled read structure, and none of these prior artwork has used a single transistor decoupled read.

The write mode of the proposed SRAM is as following. At first phase, when WWL is High and W WL is Low level, MOS transistors: MN4, MN5, MP3, and MP4 are ON. Hence, the node x and x is possible to change the write-mode, and then MN3 is OFF in order to reduce the energy dissipation in the elementary cell. In second phase, adiabatic signal line

V. Alternative SRAM Design With Adiabatic Logic

The elementary cell of proposed circuit consists of two high load resistors which is constructed of PMOS (MP1 and MP2), and a cross-coupled NMOS pair (MN1 and MN2). In order to reduce the energy dissipation in the elementary cell, the PMOS having off-leak current is used. Using the PMOS as a high resistor the cell area can be small compared with the conventional 4T-SRAM using poly resistor. NMOS switch (MN3) is necessary to restrict a short circuit current when the data is written in the elementary cell. In the proposed circuit, decreasing signal voltage on the write (or read) line is limited by transmission gate; however normal NMOS switch is better from the viewpoint of cell area if voltage drop is no problem.

The write mode of the proposed SRAM is as following. At first phase, when WWL is High and W WL is Low level, MOS transistors: MN4, MN5, MP3, and MP4 are ON. Hence, the node x and x is possible to change the write-mode, and then MN3 is OFF in order to reduce the energy dissipation in the elementary cell. In second phase, adiabatic signal line

VI. SRAM Design With St Inveter

The overall power dissipation will depends on the supply voltage scaling. If there is any reduction present in the supply voltage then there will be reduction in the dynamic power and the leakage power quadratic ally and linearly (to the first order) respectively. By the reduction in the supply voltage, the sensitivity of circuit parameters to process variations will get increase. This causes to limit the circuit operation in the low-voltage regime and particularly for SRAM bit cells employing minimum-sized transistors. The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write failure, and access-time failure. The process constraints such as gate-
oxide reliability limits are used to determine the maximum supply voltage $V_{\text{max}}$ which is used for the transistor operation. $V_{\text{max}}$ is getting reduce with the technology scaling due to scaling of gate-oxide thickness.

The minimum SRAM supply voltage ($V_{\text{min}}$) for a given performance requirement is limited by the increased process variations i.e., both random and die-to-die and the increased sensitivity of circuit parameters at lower supply Voltage. Moreover, to enable SRAM bit cell operation across a larger voltage range $V_{\text{min}}$, has to be further minimized to low. In the case of six-transistor bit cell, the SRAM $V_{\text{min}}$ can be lowered with out adding extra transistors. In this work, we focus only on various configurations of bit cell. Hence, we believe that to reduce the $V_{\text{min}}$ we apply the read-write assist circuits to these bitcell configurations.

![Fig. 7. Conceptual ST schematics: the gate connection of the feedback transistor is connected to the VCC to show the feedback mechanism during 0 to 1 input transition](image)

**A. Read-Failure Probability:**

Read static noise margin (SNM) is used to quantify the read-stability of the SRAM bit cells. The SNM is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve. Read-failure probability ($P_{\text{read-fail}}$) is estimated as $P_{\text{read-fail}} = \text{Prob. (Read SNM} < kT)$. If read SNM is lower than the thermal voltage ($kT = 26 \text{ mV at } 300 \text{ K}$), the bit cell contents can be flipped due to thermal noise. Note that any other suitable threshold criteria can be used in estimating read-failure probability. Read-$V_{\text{min}}$ is determined at the 6-sigma read-failure probability (i.e $P_{\text{read-fail}} = 1e^{-9}$).

**B. Hold-Failure Probability:**

Similar to the read stability case, hold-stability is estimated by computing the hold SNM. Fig. 8 shows the hold-failure probability variation versus supply voltage for 6T and ST bit cells. As shown in inset, hold-failure probability ($P_{\text{hold-fail}}$) is estimated as

$$P_{\text{hold-fail}} = \text{Prob. (hold SNM} \times kT)$$

Hold-$V_{\text{min}}$ is determined at the 6-sigma hold failure probability (i.e., $P_{\text{hold-fail}} = 1e^{-9}$). It is observed that upsizing 6T device dimensions give robust inverter characteristics. This gives lower hold-failure probability and lower hold-$V_{\text{min}}$ compared to the minimum sized ST-1 and ST-2 bit cells. Note that ST-1 bit cells having internal node-based feedback give improved hold-failure characteristics compared with the ST-2 bit cell.

![Fig. 8. Proposed SRAM with ST inverter](image)

**C Write-Failure Probability:**

Write-ability of a bit cell gives an indication of how easy or difficult it is to write to the bit cell. Fig. 9.1 shows the write failure probability variation versus supply voltage. As shown in inset, write-failure probability ($P_{\text{write-fail}}$) is calculated as

$$P_{\text{write-fail}} = \text{Prob. (write-trip-point} < 0 \text{ mV})$$

**VII. Simulation Result**

The conventional SRAMs and the proposed SRAM are tested by SPICE simulation using a 22 $\mu$m standard CMOS process technology. The parameters of the proposed circuit and simulation conditions are summarized in Table I. To evaluate the power savings in the circuits, we compute the energy consumption $E$, which is defined as follows:

$$E = \int_{0}^{T_{s}} \left( \sum_{i=1}^{n} (V_{i, p}(t)) \right) dt.$$

... (1)

![Fig. 9.1 Simulation results of existing system](image)

The following Fig. 9.2 explains the proposed system of Schmitt triggered based SRAM simulated w-edit waveform.
VIII. Conclusion:

In this paper, we have presented an adiabatic SRAM. The proposed SRAM has used two trapezoidal wave pulses and has been controlled switching current flow. Our simulation result with the proposed circuit has indicated a factor of 14 over reductions in energy consumption. Lowering the supply of voltage is an effectiveness way to achieve ultra-low-power operation. In this work, we evaluated ST-based SRAM bit cells suitable for ultra-low-voltage applications. The built-in feedback mechanism in the proposed ST bit cell can be effective for process-tolerant, low-voltage SRAM operation in future nano-scaled technologies. Monte Carlo simulations in 65-nm technology predict lower for the proposed ST-2 bit cell under the iso area condition. Measurement results with a 130-nm test-chip clearly demonstrate the effectiveness of the proposed ST-2 bit cell for successful ultralow-voltage operation.

The following table explains the power comparison for different SRAM design approaches.

<table>
<thead>
<tr>
<th></th>
<th>POWER DISSiPATION</th>
<th>DELAY</th>
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<tbody>
<tr>
<td>CMOS 6T SRAM</td>
<td>2.36903×10^-4 watts</td>
<td>0.25</td>
</tr>
<tr>
<td>HETT 6T SRAM</td>
<td>4.128965×10^-5 watts</td>
<td>0.47</td>
</tr>
<tr>
<td>7T SRAM</td>
<td>5.3923×10^-3 watts</td>
<td>1.98</td>
</tr>
<tr>
<td>7T SRAM ARRAY</td>
<td>2.53334×10^-2 watts</td>
<td>1.20</td>
</tr>
<tr>
<td>6T SRAM ADIABATIC LOGIC</td>
<td>4.70454×10^-4 watts</td>
<td>0.43</td>
</tr>
<tr>
<td>5T SRAM USING ST</td>
<td>7.37457×10^-5 watts</td>
<td>0.58</td>
</tr>
</tbody>
</table>

Table 1 Power Consumption of different SRAM design

IX. Future Work

In this paper, 6T/ST SRAM bit cell topologies are analyzed for achieving low voltage operation. ST bit cells offer low voltage operation with 2 area overhead. On the other hand, various read/write assist techniques achieve significant reduction, with lower area overhead. Hence, for a given constraint, optimal combination of the bit cell topology read/write assist technique should be chosen for minimal area/power overhead. Thus, the effectiveness of read/write assist techniques for each of the bit cell topology needs to be investigated for achieving lower.

References


Authors Profile

Suganya.S has received her B.E. degree in Electronics and communication engineering at kings college of engineering under Anna university, Chennai. Currently pursuing her M.Tech Degree in Sathyabama University. Area of interest is reversible logic, quantum electronics and RF-ID, has presented papers in various national and international conferences.

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